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(51) Int. Cl.⁵: **H04N 5/45, H04N 5/44**

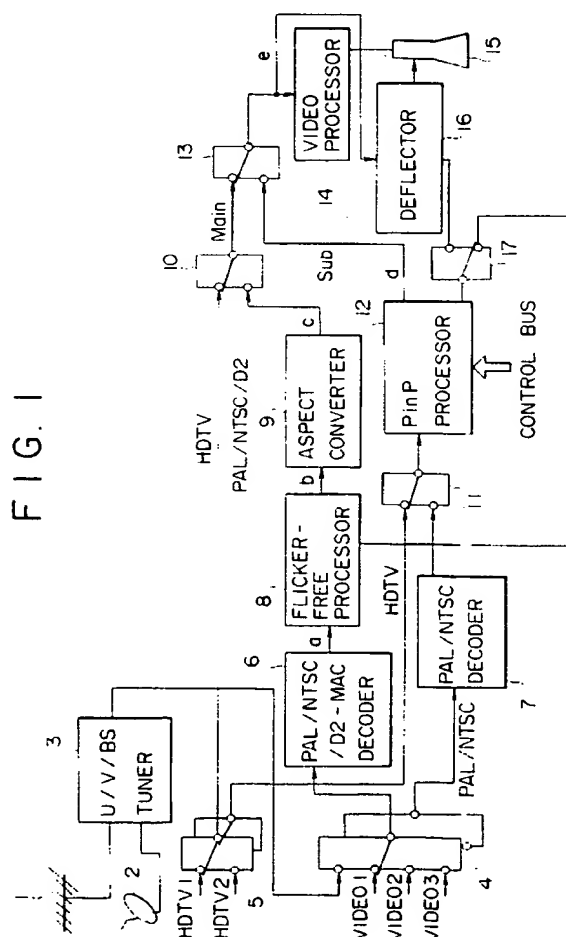
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(57) A display apparatus comprising a field frequency converter for converting the field frequency of a parent-picture video signal; an aspect ratio converter for converting the aspect ratio of the video signal posterior to the field frequency conversion; a child-picture processor for generating a child-picture video signal; and a switch for synthesizing the aspect-converted video signal with the video signal obtained from the child-picture processor. In this constitution, the storage capacity of a memory required in the field frequency converter can be minimized. The apparatus further comprises a selector for selecting either the parent-picture video signal of the second aspect ratio or the parent-picture video signal of which first aspect ratio has been converted to the second aspect ratio, wherein merely one switch is sufficient for synthesizing the video signal obtained from the child-picture processor with the selected parent-picture video signal of the second aspect ratio.



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The present invention relates to a display apparatus having a picture-in-picture or picture-out-picture function for superimposing a sub picture on a main picture being displayed on a screen of a television receiver or the like.

Fig. 12 of the accompanying drawings shows some examples where a sub picture is displayed in a predetermined area of a main picture. In Fig. 12 (A), a main picture is displayed in a left portion of a screen, and one sub picture is displayed at its lower right end. Next in Fig. 12 (B), there are displayed three sub pictures of individually different channels. In this example, the images of three channels are visually represented as indexes. The display method employed in the above two examples is generally termed PoutP (picture-out-picture) since any sub picture is positioned at the end portion of the main picture.

Fig. 12 (C) and (D) show another display method termed PinP (picture-in-picture). In the example (C), a main picture is displayed in a zoom mode with its upper and lower end portions cut, and a sub picture is displayed with partial insertion in the lower right area of the main picture. Further in the example (D), sub pictures are displayed at the four corner areas of the main picture respectively.

Fig. 13 is a circuit block diagram of a conventional display apparatus for superimposing a sub picture on a parent-picture as mentioned. In this example, a mixer 101 mixes a sub picture signal with a main picture signal and supplies the mixed signal to an aspect ratio converter 102. Then the aspect ratio converter 102 converts the aspect ratio of the input signal and supplies its output to a double speed converter 103, which converts the input video signal into a double speed signal and outputs the same to a mixer 105 via a switch 104. Subsequently the mixer 105 delivers the input video signal from the double speed converter 103 directly as an output, or mixes a sub picture signal with the input main picture signal of HD-MAC format received via the switch 104 and then outputs the mixed signal therefrom.

Now the operation of the above conventional apparatus will be described below with reference to a timing chart of Fig. 14. The mixer 101 is supplied with the parent-picture and child-picture video signals of the PAL or NTSC system. The substantial picture signal included in such composite video signal is so set as to have, e.g., 720 pixels per horizontal scanning period H. The mixer 101 curtails the pixels of the sub picture to, e.g., 240. The data of the 240-pixel sub picture (Fig. 14(b)) is inserted in a predetermined region of the 720-pixel main picture (Fig. 14(a)) to thereby produce a new video signal (Fig. 14(c)).

The data thus obtained is converted by the aspect ratio converter 102 into a signal of a desired aspect ratio. More specifically, in case the aspect ratio of a display unit (not shown) connected to the rear stage of the mixer 105 is 16:9, the video signal of an

aspect ratio 4:3 supplied from the mixer 101 is converted into a video signal of an aspect ratio 16:9 (Fig. 14(d)). The converted video signal is inputted to the double speed converter 103, which then produces a video signal of a double field frequency converted as shown in Fig. 14(e). The video signal thus produced is supplied via the switch 104 to the mixer 105, from which the signal is directly outputted to and represented visually on the display unit.

Fig. 15 shows the principle of such double speed conversion. The PAL or NTSC video signal is in a 2:1 interlaced format of 625 lines at 50 Hz, and its aspect ratio is set to 4:3. The one-frame video signal of 625 H consists of two video signals of an odd field and an even field each composed of 312.5 H. The double speed converter 103 produces, out of the odd-field video signal, two double-frequency odd-field video signals of 313H and 312.5H. The converter 103 further produces two even-field video signals of 312H and 312.5H by doubling the frequency of the even-field signal of 312.5H.

Consequently, as shown in Fig. 16, the odd-field video signal of 312.5H is displayed in succession to the odd-field video signal of 313H. Subsequently the even-field video signal of 312H is displayed, which is followed by the even-field video signal of 312.5H. Since the field frequency is doubled as mentioned, it becomes possible to prevent occurrence of flicker.

Meanwhile the HD-MAC video signal based on the European HD TV standard is in a 2:1 interlaced format of 1250 lines at 50 Hz, and its aspect ratio is set to 16:9. In case the HD-MAC video signal is used for a main picture, it is impossible to employ the mixer 101 in common to the PAL or NTSC system and the HD-MAC system since the number of lines in the former and that in the latter are fundamentally different from each other. Therefore, in using the HD-MAC video signal for a main picture, the circuit configuration is so contrived that the parent-picture video signal is supplied to the mixer 105 via the switch 104, and a child-picture child-picture signal is mixed with the parent-picture signal in the mixer 105.

In displaying a sub picture to a main picture in the PoutP mode, a child-picture video signal of 240 pixels is added to a parent-picture video signal of 720 pixels, as shown in Fig. 17(a). It follows therefrom that the length of the mixed signal is rendered greater than the length of 1H. Accordingly, for double speed conversion of such signal, there exists the necessity of providing two field memories in the double speed converter and writing the data therein alternately per line. For this purpose, memories with a capacity for the data of two fields are required, which raises a problem with regard to an increase of the production cost. In an attempt to eliminate such disadvantage, the video signal shown in Fig. 17(a) may be so processed that its aspect ratio is converted as shown in Fig. 17(b) to remove the overlap on the time base,

and then double speed conversion is executed. This process enables a single field memory to be sufficient for the double speed conversion.

However, since the number of pixels of the IH data inputted to the double speed converter 103 is 960 (= 720 + 240), the storage capacity of the memory employed in the double speed converter 103 needs to be 4/3 (= 960/720) times the 720 pixels required for the display in the picture-in-picture mode. Consequently the problem of the high production cost is still left unsolved.

Furthermore, in one case of using the HD-MAC video signal for a main picture and another case of using the NTSC or PAL video signal for a main picture, the numbers of lines in such two cases are widely different from each other, fails to achieve common use of the circuit which mixes a sub picture with a main picture, whereby circuits of two systems are needed to increase the production cost.

In addition, if the frequency-converted video signals are employed for discrimination between the odd and even fields of the video signals posterior to conversion of the field frequency, it becomes necessary to discriminate among 312.5H, 313H, 312.5H and 312H to consequently require a greater circuit scale, hence causing difficulties in realization of stable discrimination.

OBJECT AND SUMMARY OF THE INVENTION

The present invention has been accomplished in view of the circumstances mentioned above, and resides in providing an improved display apparatus which is capable of reducing the storage capacity of a memory required for field frequency conversion and of reducing the number of mixer circuits with another advantage of ensuring stable discrimination between even and odd fields.

According to a first aspect of the present invention, there is provided a display apparatus comprising a field frequency converter means, preferably a flicker-free processor, for converting the field frequency of a parent-picture video signal; an aspect ratio converter means for converting the aspect ratio of the video signal of which field frequency has been converted by the converter means; child-picture processor means for generating a child-picture video signal; and synthesizer means, preferably a suitably controlled switch, for synthesizing the video signal of which aspect ratio has been converted by the aspect converter, and the video signal obtained from the child-picture processor. In this display apparatus, the field frequency of the parent-picture video signal is converted by the frequency converter, and then the child-picture video signal is synthesized therewith. Consequently the storage capacity of the memory required in the processor can be minimized.

According to a second aspect of the present in-

vention, there is provided a display apparatus comprising a field frequency converter means, preferably a flicker-free processor, for converting the field frequency of a parent-picture video signal having a first aspect ratio of, e.g., 4:3; an aspect ratio converter means for converting the aspect ratio 4:3 of the video signal, of which the field frequency has already been converted by the converter means, to a second aspect ratio of, e.g., 16:9; a selector means, preferably a switch, for selecting either the parent-picture video signal of the aspect ratio 16:9 or the parent-picture video signal of which the aspect ratio has been converted by the aspect converter from 4:3 to 16:9; and a synthesizer means, preferably a suitably controlled switch, for synthesizing the video signal obtained from the processor with the video signal of the aspect ratio 16:9 selected by the first-mentioned switch. In this display apparatus, first the aspect ratio of the parent-picture video signal is converted by the aspect converter, and then the child-picture video signal obtained from the processor is synthesized with the parent-picture video signal. Therefore, any desired video signal of the aspect ratio 16:9 can be selected by the first-mentioned switch and supplied to the synthesizer switch. As a result, merely one switch is sufficient for synthesizing the sub picture with the main picture.

According to a third aspect of the present invention, there is provided a display apparatus comprising a field frequency converter means, preferably a flicker-free processor, for converting the field frequency of a parent-picture video signal; storage means for storing a child-picture video signal; synthesizer means, preferably a switch, for synthesizing the child-picture video signal read out from the storage means with the parent-picture video signal of which the field frequency has already been converted; a field detector means for detecting the odd fields and the even fields with respect to the parent-picture video signal prior to the field frequency conversion; and a processor for controlling the reading from memories of the storage means in accordance with the output of the detection circuit. In this display apparatus, discrimination between the odd fields and the even fields can be executed on the basis of the parent-picture video signal prior to the field frequency conversion. And the operation of reading out the signal from the memories is controlled in accordance with the result of such discrimination. Consequently the discrimination between the odd and even fields can be performed with accuracy, and the circuit configuration for such control can be simplified.

The invention will be further described by way of non-limitative example with reference to the accompanying drawings, in which:-

Fig. 1 is a block diagram of an embodiment of display apparatus according to the present invention;

Fig. 2 is a timing chart of signals for explaining the

operation of the embodiment shown in Fig. 1;

Fig. 3 is a block diagram of a PinP processor employed in the embodiment of Fig. 1;

Fig. 4 is a timing chart of signals for explaining the operation of the PinP processor shown in Fig. 3;

Fig. 5 is a block diagram of a reading circuit configuration of the PinP processor employed in the embodiment of Fig. 1;

Fig. 6 is a timing chart of signals for explaining the operation of the PinP processor shown in Fig. 5;

Fig. 7 is another timing chart of signals for explaining the operation of the PinP processor shown in Fig. 5;

Fig. 8 is a further timing chart of signals for explaining the operation of the PinP processor shown in Fig. 5;

Fig. 9 is a block diagram showing the constitution of a detector included in the PinP processor of Fig. 1;

Fig. 10 is a timing chart of signals for explaining the operation of the detector shown in Fig. 9;

Fig. 11 is another timing chart of signals for explaining the operation of the detector shown in Fig. 9;

Fig. 12 (A) through (D) illustrate examples of display modes where a sub picture is superimposed on a main picture;

Fig. 13 is a block diagram of an exemplary conventional display apparatus;

Fig. 14 is a timing chart of signals for explaining the operation of the display apparatus shown in Fig. 13;

Fig. 15 is another timing chart of signals for explaining the operation of the display apparatus shown in Fig. 13;

Fig. 16 illustrates scanning lines in the conversion of a field frequency in the apparatus of Fig. 13; and

Fig. 17 illustrates signals in a PoutP display mode.

Fig. 1 is a block diagram showing the constitution of an exemplary embodiment which represents the display apparatus of the present invention. An antenna 1 serves to receive UHF and VHF television broadcast waves, while an antenna 2 serves to receive satellite broadcast waves. A tuner 3 receives the outputs of the antennas 1, 2 and supplies its detected output to one input terminal of a switch 4, to which are also supplied, in addition to the output of the tuner 3, video signals 1 through 3 from an unshown VTR or the like. The switch 4 selects one of the inputs supplied thereto and delivers the selected signal to decoders 6 and 7.

The decoder 6 decodes the parent-picture video signal supplied from the switch 4 and outputs the decoded signal to a flicker-free processor 8. In this embodiment, the decoder 6 is so formed as to be capable of decoding any of PAL, NTSC and D2-MAC video

signals. The flicker-free processor 8 serves to double the field frequency of the video signal supplied from the decoder 6 and outputs the frequency-converted signal. And an aspect converter 9 converts the aspect ratio of the input frequency-doubled video signal to 16:9 in case the ratio thereof is 4:3. When the aspect ratio of the input video signal is 16:9, the signal is outputted directly without any conversion of the aspect ratio.

A switch 5 selects one of HD TV signals of the HD-MAC format and so forth supplied from an unshown apparatus, and outputs the selected signal to switches 10 and 11. The switch 10 selects either the video signal supplied from the switch 5 or the video signal from the aspect converter 9, and supplies the selected signal to one input terminal of a switch 13. More specifically, the aspect ratio of the video signal supplied to each input terminal of the switch 10 is so processed as to be 16:9. Therefore the video signal supplied to one input terminal of the switch 13 always has an aspect ratio of 16:9.

Meanwhile the decoder 7 decodes the video signal selected by the switch 4 and supplies the selected signal to the other input terminal of the switch 11. As described above, the HD TV video signal selected by the switch 5 is supplied to one terminal of the switch 11. Therefore the switch 11 selects one of the input signals and outputs the same to the PinP processor 12, which then generates a child-picture video signal from the input video signal. For generating such child-picture video signal, the processor 12 detects a vertical synchronizing signal and a vertical synchronizing signal from the parent-picture video signal supplied thereto via the switch 10.

The child-picture video signal obtained from the processor 12 is supplied to the other input terminal of the switch 13. The switch 13 is changed at a predetermined timing to the upper or lower position in Fig. 1 and synthesizes the child-picture video signal, which is supplied from the processor 12, with the parent-picture video signal obtained from the switch 10, and then delivers the synthesized signal to a video processor 14. Subsequently the video signal processed by the video processor 14 is outputted to and displayed on a CRT 15 which has an aspect ratio of 16:9.

A deflector 16 detects the vertical and horizontal synchronizing signals from the output of the switch 13 and controls the scanning on the CRT 15 in accordance with the detected signals. A switch 17 selects the vertical and horizontal synchronizing signals included in the video signal outputted from the flicker-free processor 8 or the deflector 16 prior to the field signal conversion and delivers the selected signals to the processor 12.

In this embodiment, the main picture video signal is supplied to the switch 10 via the decoder 6, the processor 8 and the aspect converter 9, or directly from the switch 5 without being passed through any

of such circuits. And the child-picture video signal is processed by the processor 12 independently of the main picture. Therefore, no fundamental difference is existent between the operation in the PinP mode and that in the PoutP mode, and the difference is concerned merely with the switching timing of the switch 13.

Fig. 2 is a timing chart for explaining the one-line operation in synthesizing the child-picture video signal with the parent-picture video signal. The parent-picture video signal shown in Fig. 2(a) is such that the number of pixels during the time of the effective video signal out of the 1H period is set to 720. Such video signal is supplied from the decoder 6 to the processor 8, which then converts the input signal into a video signal of Fig. 2(b) having a double field frequency. This frequency conversion is performed by reading out the data of 720 pixels in conformity with clock pulses of a double frequency. As far as this process is concerned, there is no difference between the PinP mode and the PoutP mode as described, so that the required storage capacity of the memory incorporated in the processor 8 corresponds merely to the data of one field.

The video signal, of which field frequency has been doubled by the flicker-free processor 8, is then supplied to the aspect converter 9 where a video signal of Fig. 2(c) is produced with its aspect ratio so converted as shown. Meanwhile in the processor 12, there is generated a child-picture video signal composed of 240 pixels as shown in Fig. 2(d). The switch 13 is changed to the upper position in Fig. 1 when selecting the parent-picture video signal, or is changed to the lower position in the same diagram when selecting the child-picture video signal. Consequently, the video signal outputted from the switch 13 is such as shown in Fig. 2(e) where the effective video signal per line of the synthesized parent and sub pictures is composed of 720 pixels.

Fig. 3 shows a further detailed constitution of the processor 12 employed in the apparatus of Fig. 1. The luminance (Y) signal in the child-picture video signal outputted from the switch 11 is supplied to an A-D converter 21 and, after analog-to-digital conversion, the resultant digital signal is written pixel by pixel in memories 23 and 24 alternately. Meanwhile the colour difference signals PB and PR are supplied to an A-D converter 22 and, after analog-to-digital conversion, the digital signals are written in a memory 25. The child-picture horizontal synchronizing signal is supplied to a write-side PLL 26, which then generates write clock pulses of a frequency 14.3 MHz in synchronism with the horizontal synchronizing signal. A processor 40 controls the operation of writing in the memories 23 to 25 in synchronism with the write clock pulses obtained from the PLL 26. To the memories 23 to 25, there are inputted the data of 320 lines each composed of 256 pixels. And each of such pixels con-

sists of 6 bits.

Meanwhile a read-side PLL 27 generates pulses of a frequency 28.6 MHz (double the frequency of the write clock pulses generated by the write-side PLL 26) synchronized with the horizontal synchronizing signal included in the parent-picture video signal inputted from the switch 17, and then supplies such double-frequency pulses to the processor 40, to which the vertical synchronizing signal of the parent-picture video signal is also supplied from the switch 17. The processor 40 reads out the data from the memories 23 to 25 in synchronism with the input signals. Out of the data thus read, the luminance signal component is supplied to a D-A converter 28 and, after digital-to-analog conversion, the luminance signal is outputted therefrom. The colour difference signal PB is supplied to a D-A converter 29 for digital-to-analog conversion, while the other colour difference signal PR is supplied to a D-A converter 30 for digital-to-analog conversion. The signals thus converted are outputted from the converters 29 and 30 respectively.

When the first pixel data of the luminance signal is written in the memory 23 for example, the next second pixel data thereof is written in the memory 24. Thereafter the luminance signal is written pixel by pixel alternately in such a manner that the third pixel data is written in the memory 23, and then the fourth pixel data in the memory 24. Consequently, as shown in Fig. 4(C), the first-frame data is composed of the first-field data of 128 dots x 160 lines written in the area 1 and the second-field data of 128 dots x 160 lines written in the area 2. Similarly, the second-frame data is composed of the first-field data of 128 dots x 160 lines written in the area 3 and the second-field data of 128 dots x 160 lines in the area 4. Such writing operation is performed sequentially and continuously in the order of the areas 1 - 2 - 3 - 4 - 1 - 2 - 3 - 4 and so forth as shown in Fig. 4(A).

In contrast with the above, the reading operation is performed initially in the order of the areas 1 - 2 - 3 - 4 as shown in Fig. 4(B) and, after repeated reading from the areas 3 and 4, the operation is continued in the order of the areas 1 - 2 - 3 - 4 again. Due to such repeated operation of reading the data from the areas 3 and 4 twice, it becomes possible to avert a trouble that the read address passes the write address.

The operation of reading out the data of four fields is controlled in conformity with the result of discrimination between the odd and even fields performed by the detector 70 shown in Fig. 9 which will be described later. More specifically, the data are read out from the areas 1 and 3 in response to detection of the odd fields by the detector 70, or from the areas 2 and 4 in response to detection of the even fields.

Fig. 5 shows an exemplary read-side constitution of the processor 12 employed in the apparatus of Fig. 1. A read-side PLL 27 generates clock pulses syn-

chronized with the horizontal synchronizing signal included in the parent-picture video signal supplied from the switch 17. More specifically, a clock generator 54 generates clock pulses of Fig. 6(A) and supplies the same to an H counter 55, where a value -910 is initially loaded at a predetermined timing. Thereafter the clock pulses supplied from the clock generator 54 are counted, and the count is incremented by 1 per pulse. And a logical low-level signal is outputted when the count is in a range of -910 to -455, or a logical high-level signal is outputted when the count is in a range of -454 to -1, as shown in Fig. 6(B). The signal thus obtained is compared by a phase comparator 51 with the horizontal synchronizing signal included in the parent-picture video signal supplied from the switch 17. The resultant phase difference is first smoothened through a low-pass filter 52 and is supplied to a VCO (voltage-controlled oscillator) 53, which then generates clock pulses of a frequency (28.6 MHz) corresponding to the phase difference. The clock pulses thus obtained are supplied to the clock generator 54, which then generates the aforementioned clock pulses of Fig. 6(A) in synchronism with the input clock pulses.

The H counter 55 generates an HCLK signal of Fig. 6(C) whose phase is inverse to that of the signal shown in Fig. 6(B), and supplies such HCLK signal to both a V counter 56 and a V enable circuit 57. The H counter 55 further generates an H enable signal of Fig. 6(D) which is turned to a logical high level in response to a counted value of -430 to -190 or is turned to a logical low level in response to any other counted value. Such H enable signal is supplied to one input terminal of an AND gate 58.

The V counter 56 counts the HCLK signal of Fig. 7(A) supplied from the H counter 55. In the V counter 56, there is loaded a value -263 when the child-picture video signal is of the NTSC system, or a value -313 when such video signal is of the PAL system. And its count is incremented by 1 every time the HCLK signal is counted. The V counter 56 generates a VBLK signal of Fig. 7(B) which is turned to a logical high level when the counted value in the NTSC system ranges from -243 to -3 (or from -291 to -3 in the PAL system), or is turned to a logical low level when the count is any other value. This VBLK signal corresponds to the vertical blanking interval. When the counted value has reached -1, the V counter 56 generates a CARRY signal shown in Fig. 7(C).

Meanwhile the V enable circuit 57 counts the HCLK signal (Fig. 7(A)) and generates a V enable signal (Fig. 7(D)) which is turned to a logical high level when the counted value in the NTSC system ranges from -118 to -38 (or from -134 to -38 in the PAL system), or is turned to a logical low level when the count is any other value. Such V enable signal is supplied to one input terminal of an AND gate 58. Meanwhile to the other input terminal of the AND gate 58 is sup-

plied the H enable signal (Fig. 7(E)) obtained from the H counter 55, and the AND gate 58 permits the H enable signal to pass therethrough during the supply of the high-level V enable signal from the V enable circuit 57.

A timing signal generator 59 generates clock pulses SOCY1 (Fig. 8(B)) for reading out the data from the memory 23 shown in Fig. 1 during the logical high level of the H enable signal (Fig. 8(A)) supplied via the AND gate 58, and also generates clock pulses SOCY2 (Fig. 8(C)) for reading out the data from the memory 24 during the same time. Such two clock signals SOCY1 and SOCY2 are so formed that the respective phases are inverse to each other. The timing signal generator 59 further generates a signal SOE (Fig. 8(D)) which is inverse in phase to the H enable signal (Fig. 8(A)) supplied from the AND gate 58. The SOE signal is supplied from the AND gate 58. The SOE signal is supplied to the memories 23 and 24 as an enable signal to permit the data reading when its logical level is low.

Fig. 9 shows an exemplary constitution of the detector 70 included in the processor 12. The detector 70 comprises a latch circuit 71 and an inverter 72. The HCLK signal (Fig. 10(A)) generated from the H counter 55 is inputted to a terminal D of the latch circuit 71. And the vertical synchronizing signal (Fig. 10(B)) of the parent-picture video signal (prior to the field frequency conversion) outputted from the switch 17 is supplied to the inverter 72. In case the field of the main picture is an odd one, the logical level of the HCLK signal is high at the trailing-edge timing of the vertical synchronizing signal. Therefore the Q output of the latch circuit 71 is turned to a logical high level as shown in Fig. 10(C).

When the field of the parent-picture video signal is an even one, the HCLK signal (Fig. 11(A)) at the trailing edge of the vertical synchronizing signal (Fig. 11(B)) has a logical low level as shown, so that the Q output of the latch circuit 71 is turned to a logical low level. Consequently, a detection signal signifying an odd field or an even field of the parent-picture video signal is delivered from the Q output of the input circuit 71.

According to the present invention, as described hereinabove, the parent-picture video signal is synchronized with the child-picture video signal after conversion of the field frequency, so that the storage capacity of the memory means can be minimized in the process of the field frequency conversion.

Furthermore, due to the procedure of synthesizing the parent-picture video signal with the child-picture video signal after conversion of the aspect ratio, a single synthesizing means is sufficient to meet the requirement regardless of any aspect ratio of the main picture.

In addition, discrimination between odd and even fields is executed with respect to the parent-picture

video signal prior to the field frequency conversion thereof, whereby a high accuracy is attained in the discrimination with another advantage of simplifying the circuit configuration to eventually reduce the production cost of the apparatus.

Claims

1. A display apparatus comprising:
 - a field frequency converter means for converting the field frequency of a parent-picture video signal;
 - an aspect ratio converter means for converting the aspect ratio of the video signal posterior to the field frequency conversion by said field frequency converter means;
 - a child-picture processor means for generating a child-picture video signal; and
 - a synthesizer means for synthesizing the video signal of which the aspect ratio has been converted by said aspect converter means, with the video signal obtained from said child-picture processor means.
2. A display apparatus comprising:
 - a field frequency converter means for converting the field frequency of a parent-picture video signal having a first aspect ratio;
 - an aspect ratio converter means for converting the aspect ratio of the video signal, of which the field frequency has been converted by said field frequency converter means, to a second aspect ratio;
 - a selector means for selecting either the parent-picture video signal of said second aspect ratio or the parent-picture video signal of which the first aspect ratio has been converted by said aspect ratio converter means to said second aspect ratio;
 - a child-picture processor means for generating a child-picture video signal; and
 - a synthesizer means for synthesizing the video signal obtained from said child-picture processor means with the video signal of said second aspect ratio selected by said selector means.
3. A display apparatus comprising:
 - a frequency converter means for converting the field frequency of a parent-picture video signal;
 - a memory means for storing a child-picture video signal;
 - a synthesizer means for synthesizing the child-picture video signal read out from said memory means with the parent-picture video signal posterior to the field frequency conversion

thereof;

a field detector means for detecting the odd fields and the even fields with respect to the parent-picture video signal prior to the field frequency conversion thereof; and

a control means for controlling the reading from said memory means in accordance with the output of said field detector means.

FIG. 1

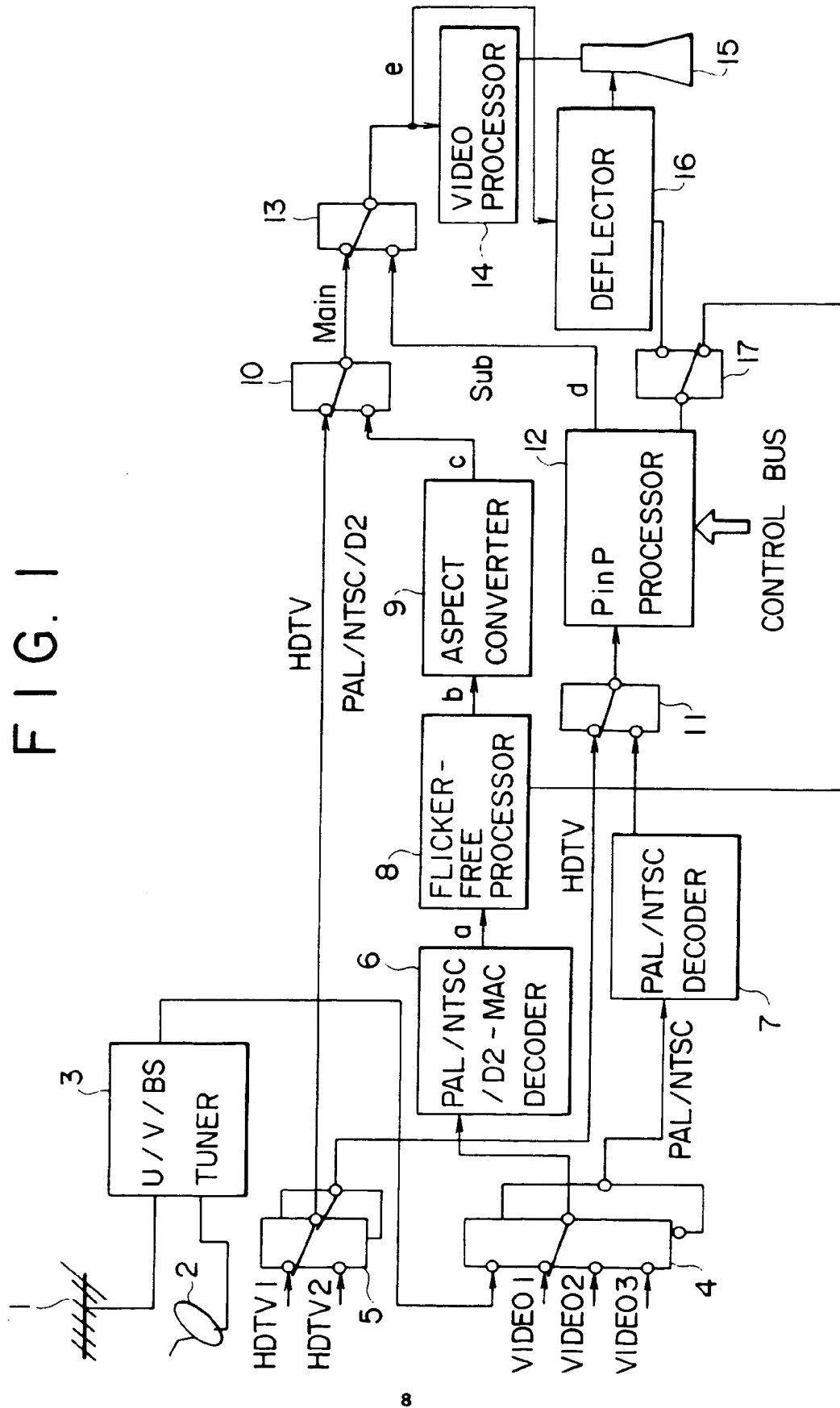


FIG. 2(a)

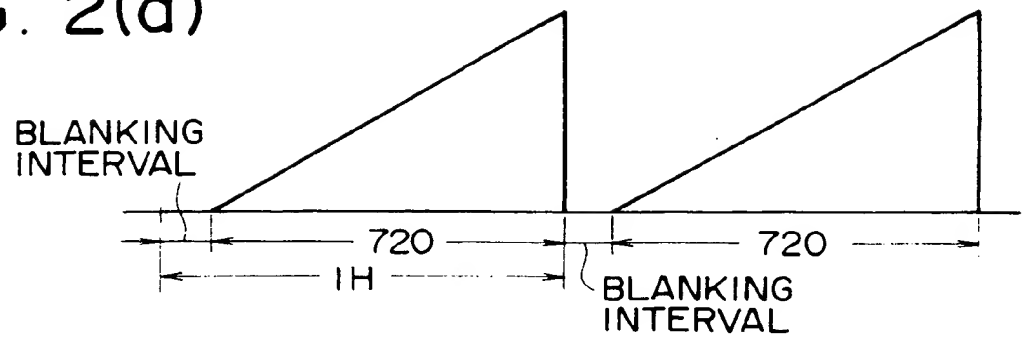


FIG. 2(b)

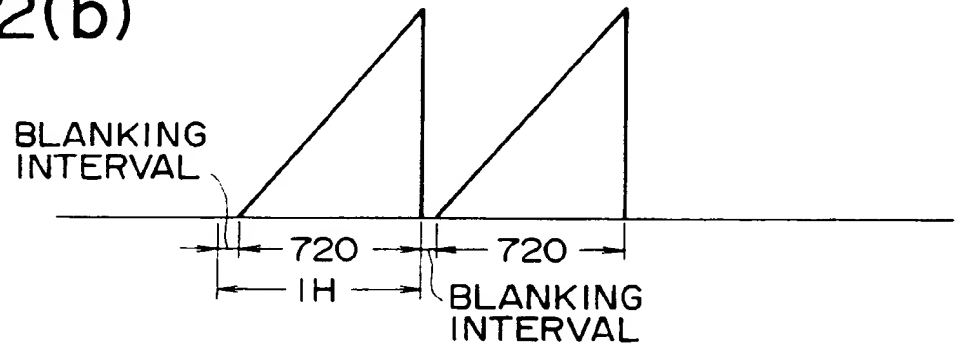


FIG. 2(c)

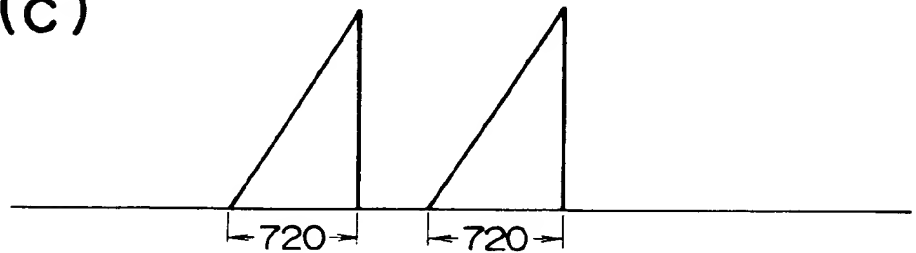


FIG. 2(d)

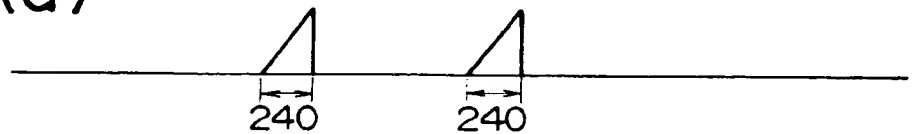


FIG. 2(e)



FIG. 3

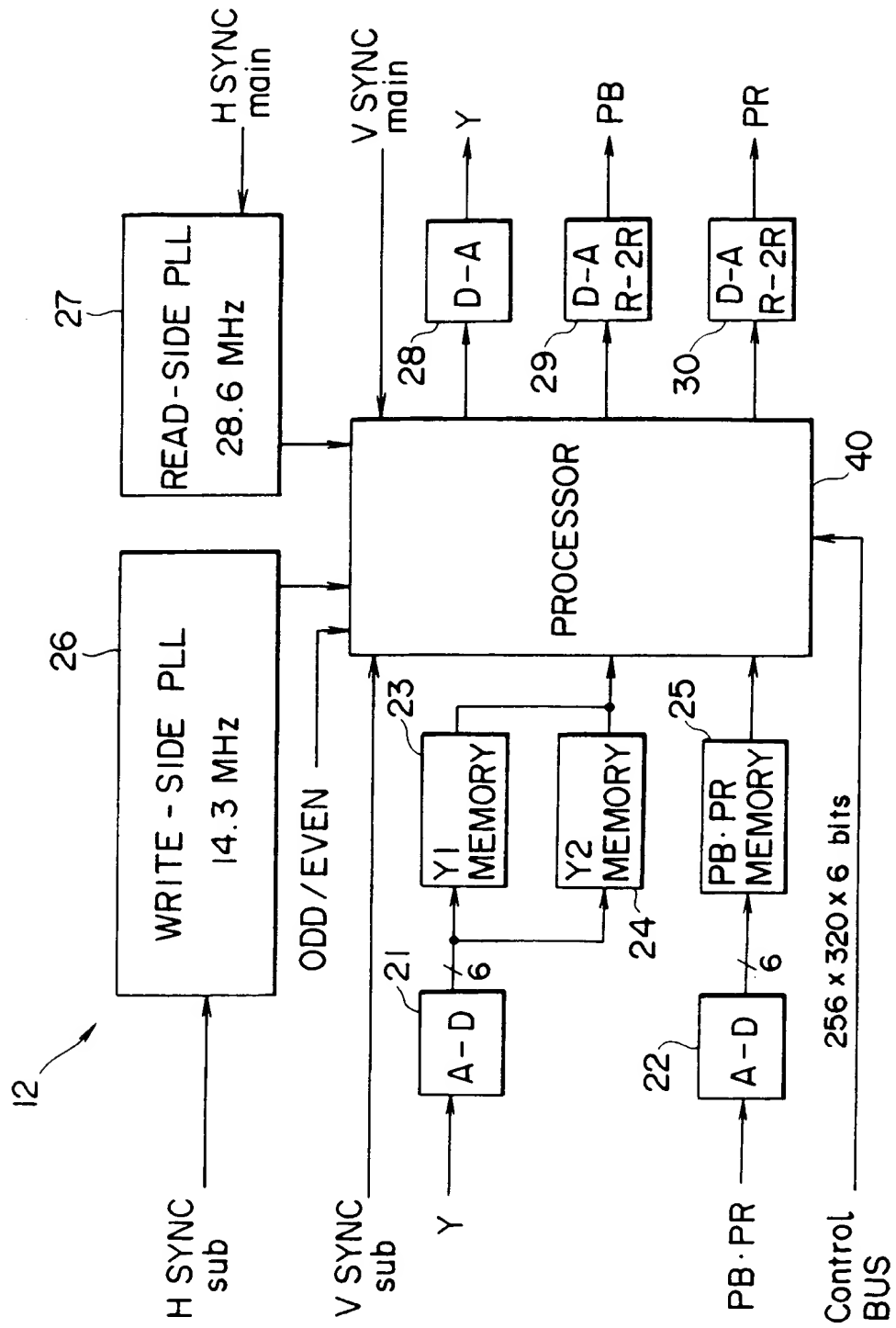


FIG. 4(A)

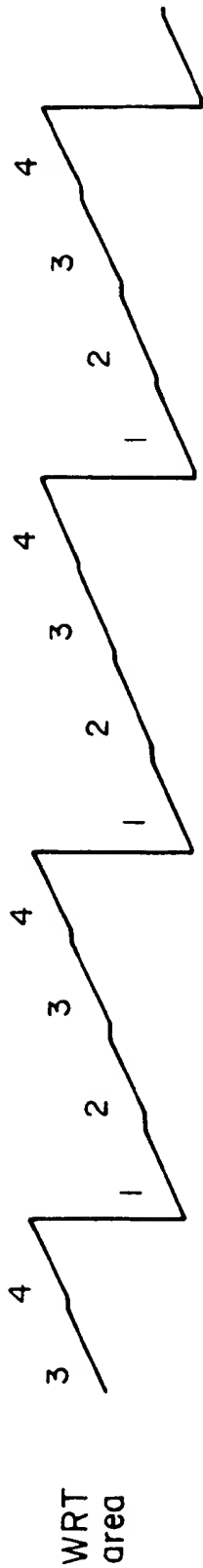


FIG. 4(B)

HOW TO AVERT PASSING OF
MEMORY ADDRESS IN AREA 3

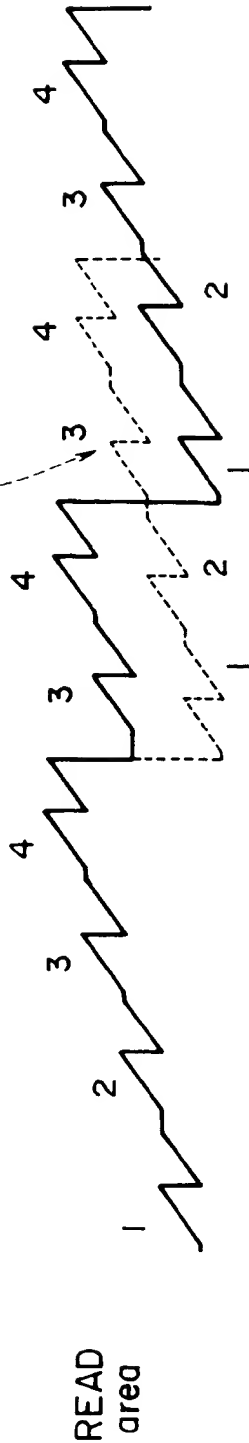


FIG. 4(C)

256 x 2 = 512 dots

1	2
3	4

MEMORY AREAS IN
4 - FIELD SEQUENCE

160 x 2 =
320 lines

FIG. 5

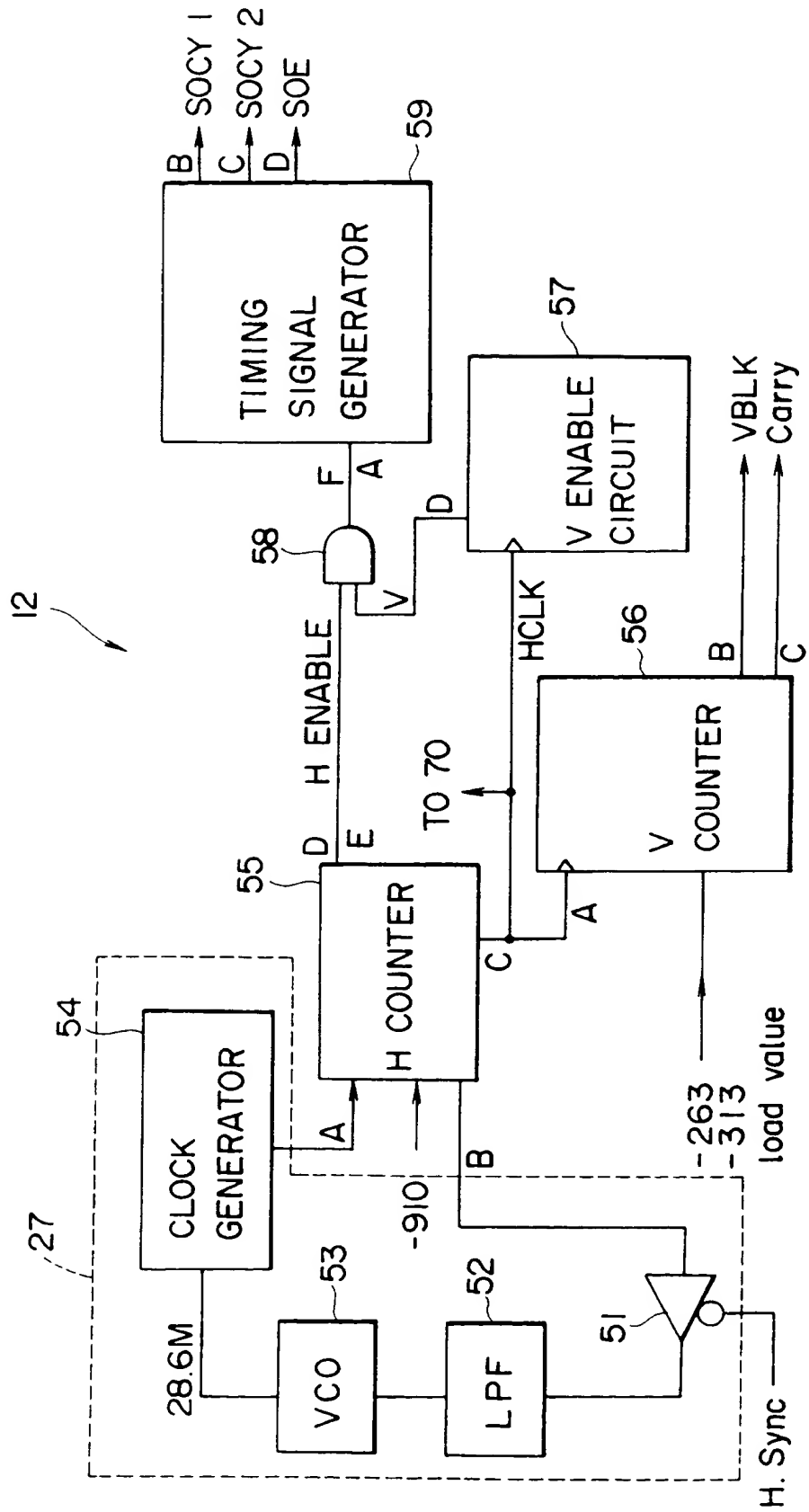


FIG. 6(A)

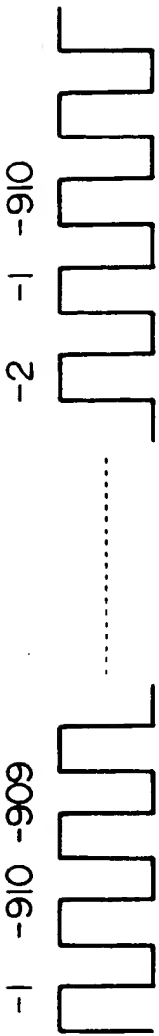


FIG. 6(B)

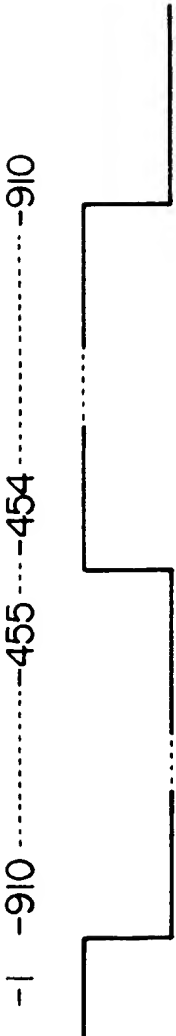
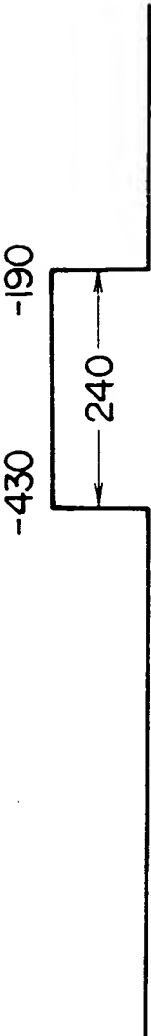


FIG. 6(C) HCLK



FIG. 6(D) H ENABLE



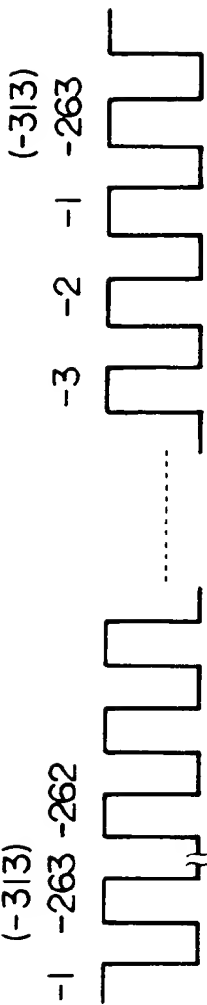


FIG. 7(A) HCLK



FIG. 7(B) VBLK

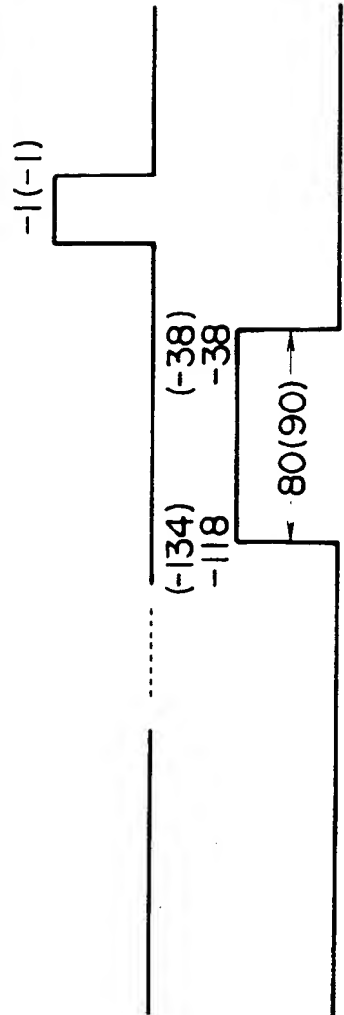


FIG. 7(C) CARRY OUT

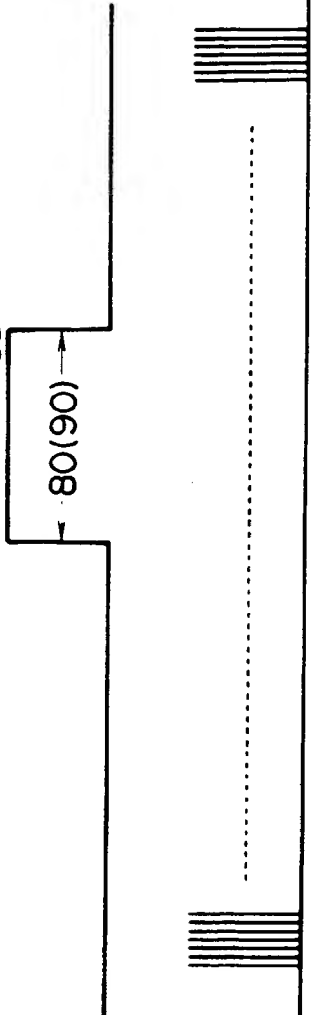


FIG. 7(D) V ENABLE

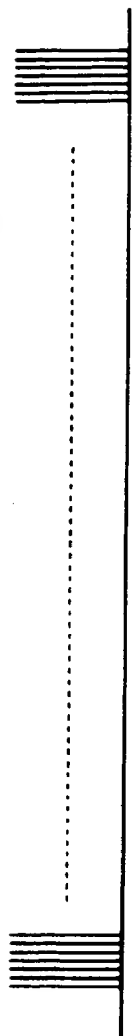


FIG. 7(E) H ENABLE



FIG. 7(F) AND

FIG. 8(A) AND



FIG. 8(B) SOCY 1

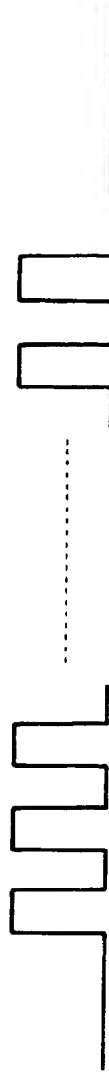


FIG. 8(C) SOCY 2

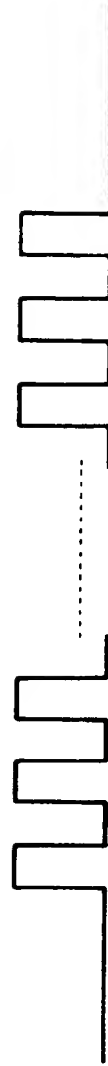


FIG. 8(D) SDE



FIG. 9

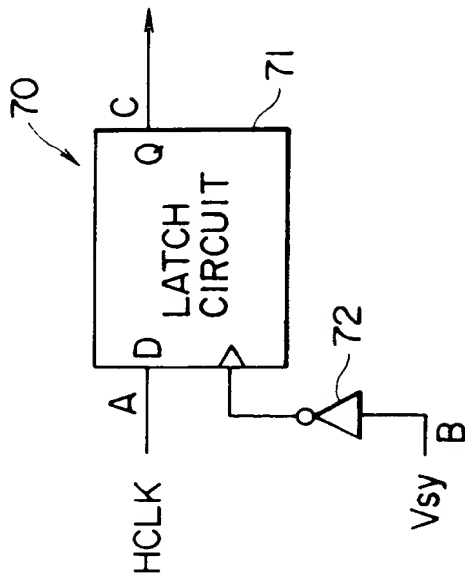


FIG. 10(A)

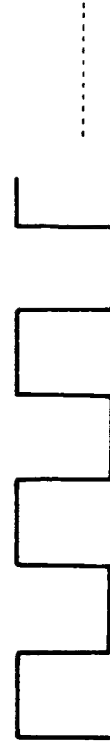
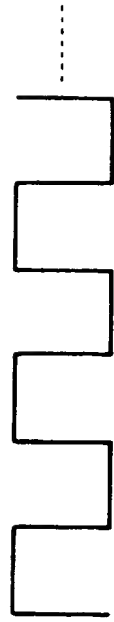


FIG. 10(B)



FIG. 10(C)





HCLK

FIG. 11(A)



Vsy

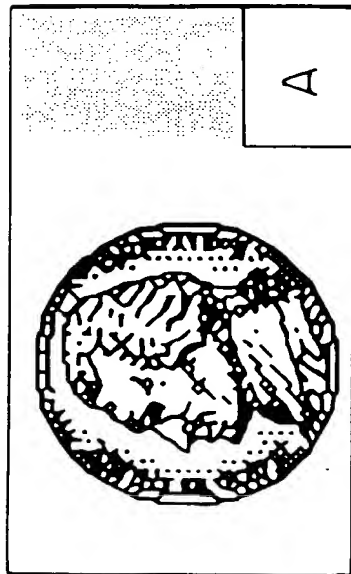
FIG. 11(B)



q

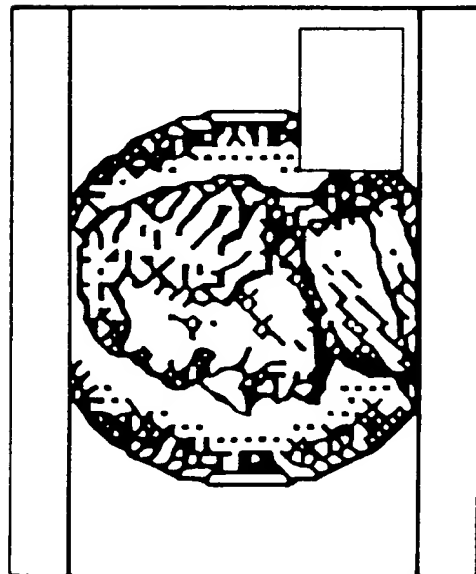
FIG. 11(C)

FIG. 12(A)



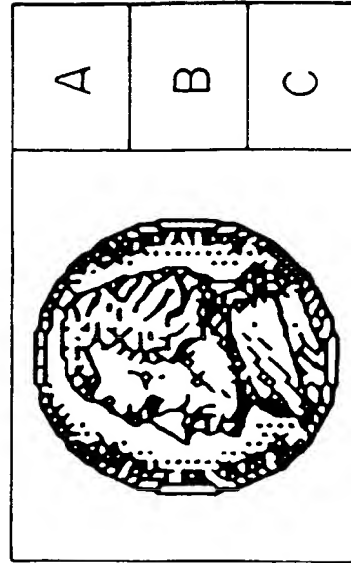
Pout P

FIG. 12(C)



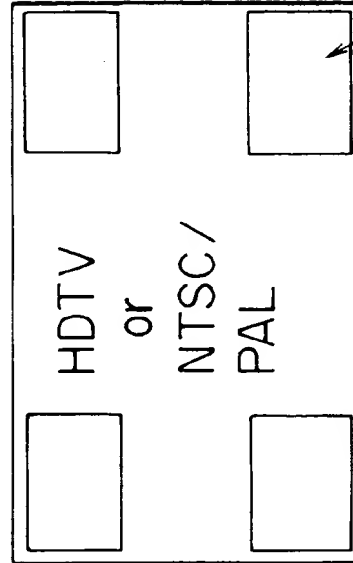
Pin P IN ZOOM MODE

FIG. 12(B)



CHANNEL INDEXES

FIG. 12(D)



4.3 OR 16.9

Pin P

FIG. 13

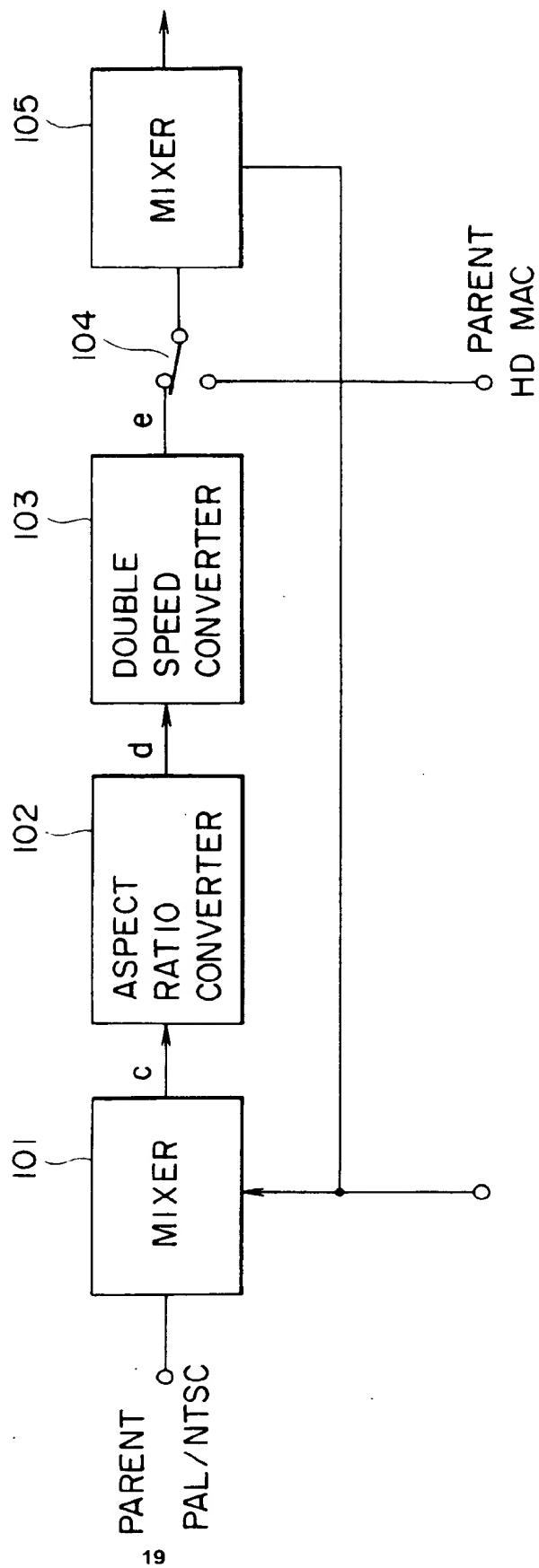


FIG. 14(a)

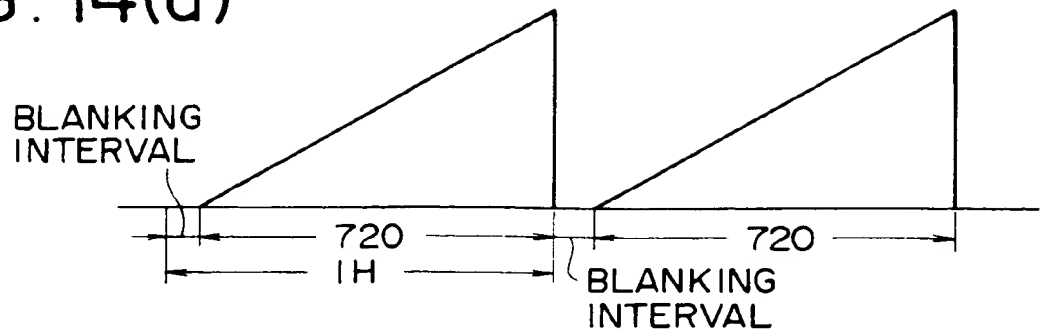


FIG. 14(b)



FIG. 14(c)

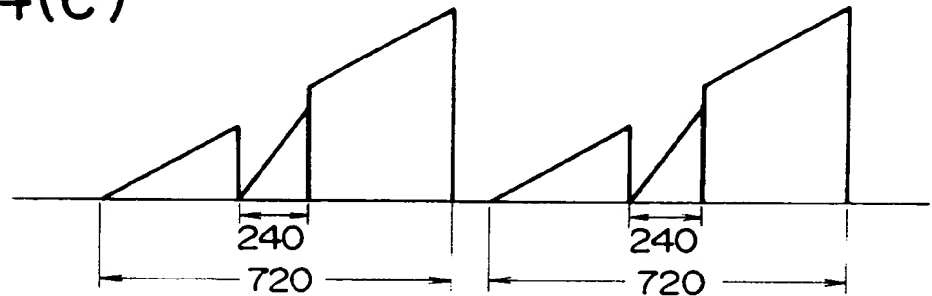


FIG. 14(d)

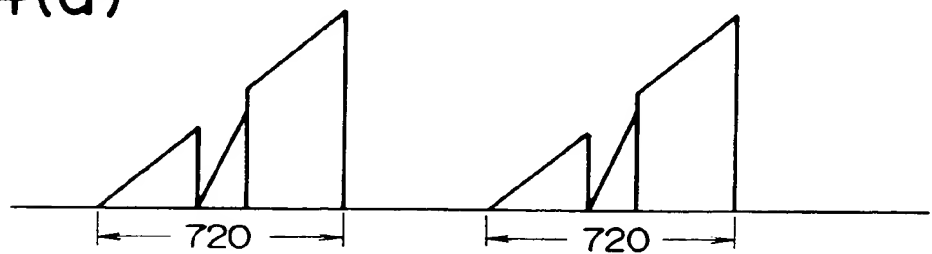


FIG. 14(e)

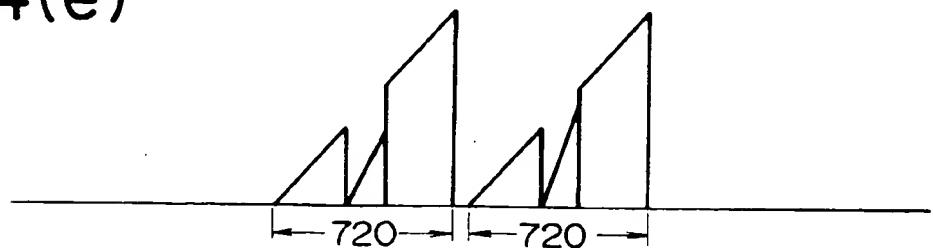
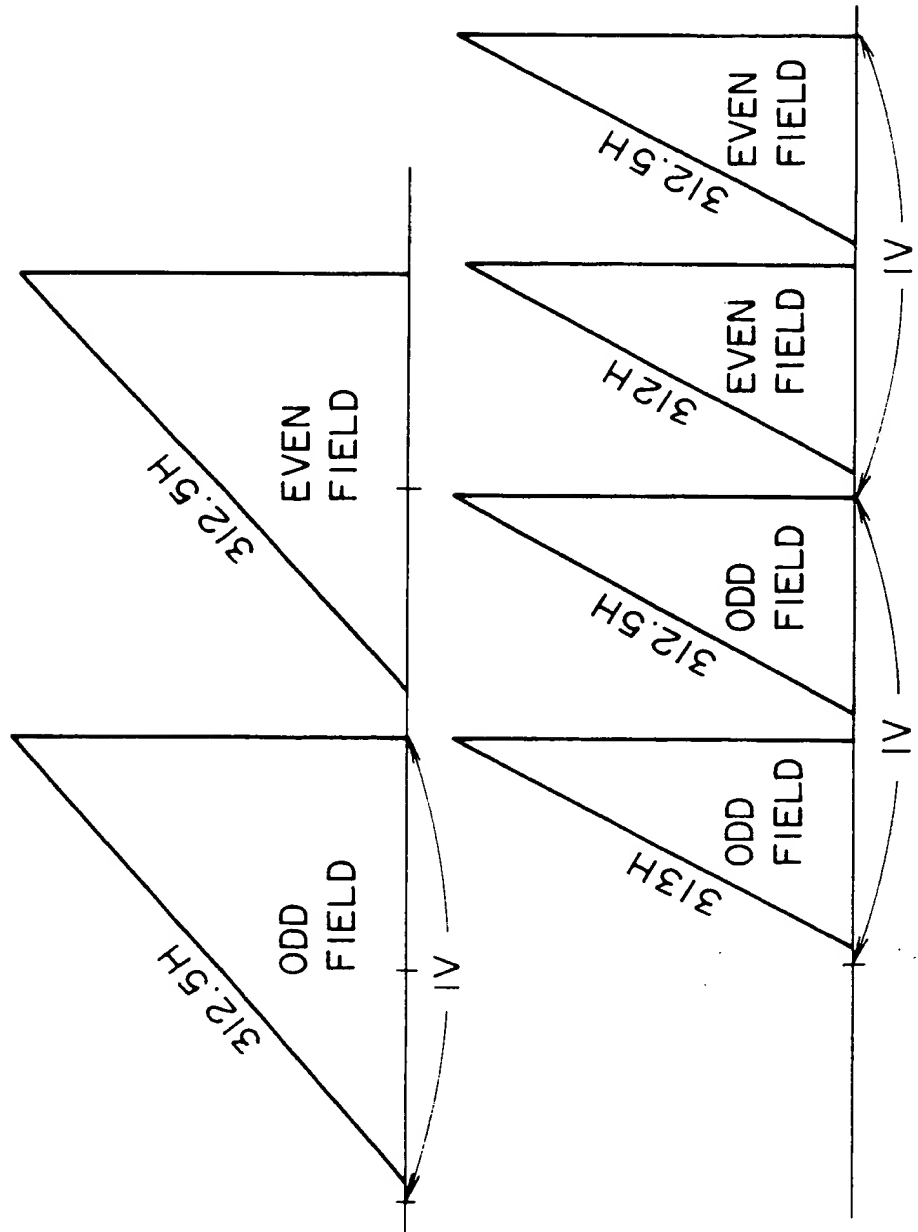
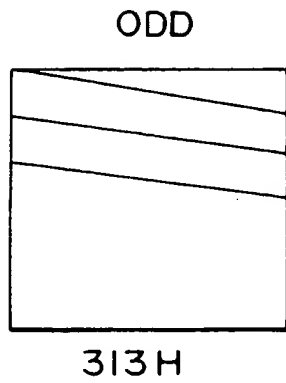


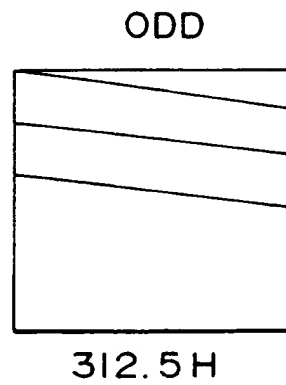
FIG. 15



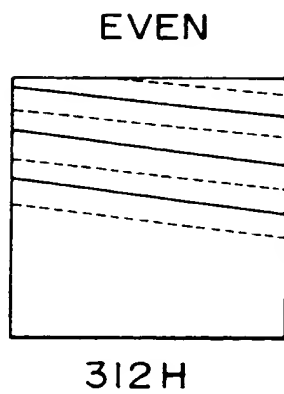
F I G. 16(a)



F I G. 16(b)



F I G. 16(c)



F I G. 16(d)

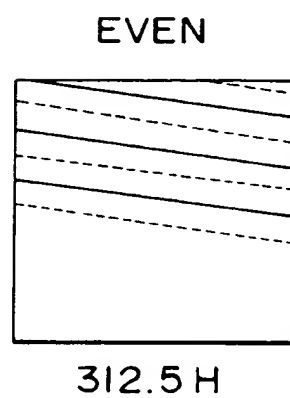


FIG. 17(a)

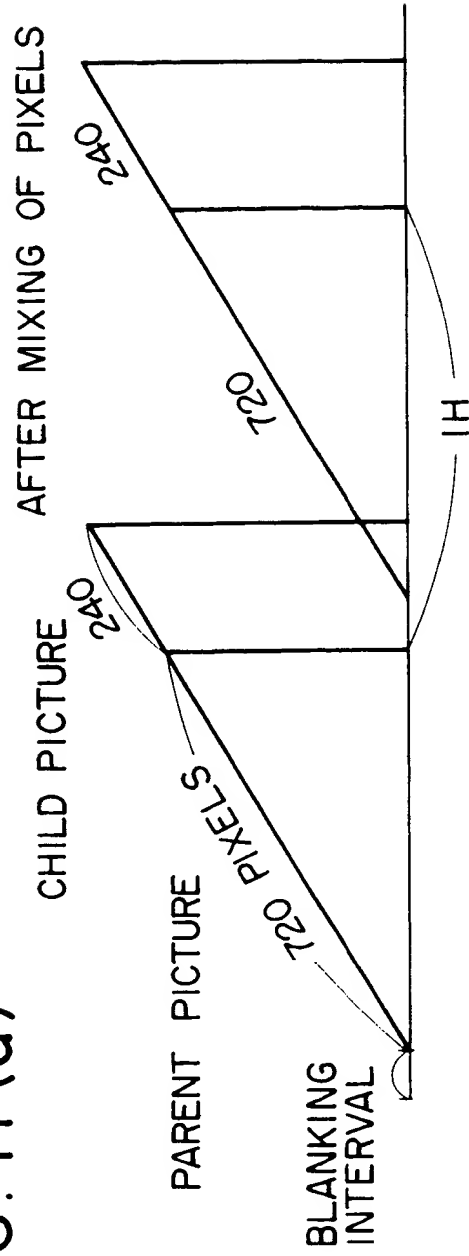
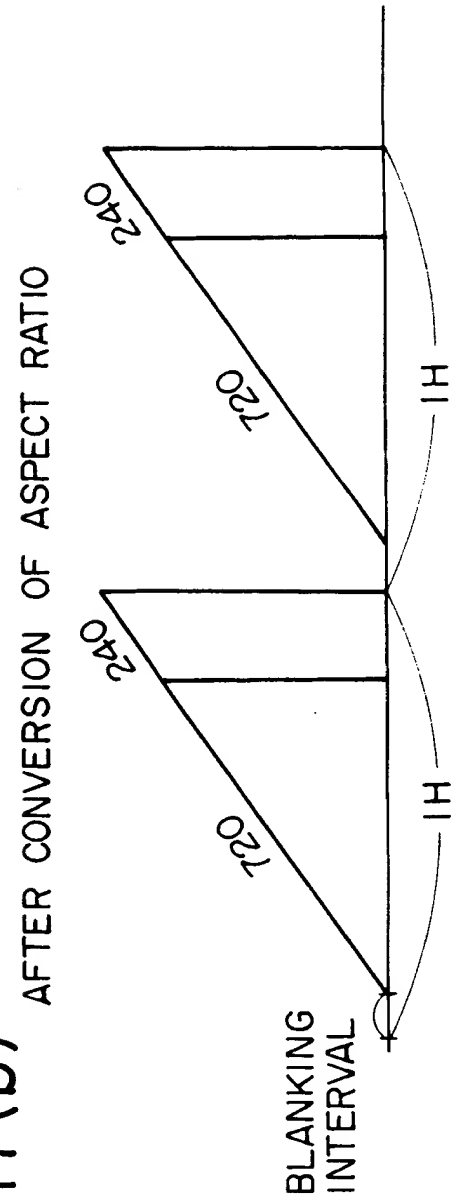


FIG. 17(b)





European Patent
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EUROPEAN SEARCH REPORT

Application Number

EP 93 30 0002

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS vol. 37, no. 3, August 1991, NEW YORK US pages 313 - 318 TSUCHIDA ET AL. 'Multi-picture system for high resolution wide aspect ratio screen' * page 313, column 2, line 1 - page 316, column 1, line 13; figures 2-4 *	1-3	H04N5/45 H04N5/44
X	IEEE 1991 INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS 5 June 1991, ROSEMONT pages 252 - 253 TSUCHIDA ET AL. 'Multi-picture system for high resolution wide aspect ratio screen' * page 1; figures 2-4 *	1,2	
A	EP-A-0 447 167 (SONY CORPORATION) * page 4, column 4, line 44 - page 5, column 5; figure 2 *	1-3	
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)
			H04N
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 31 MARCH 1993	Examiner MATERNE A.
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